Claims:

1. A magnetic memory (MRAM) device comprising:

an array of magnetic memory cells each with a magnetic data layer that can be switched between states, wherein said switching is more readily accomplished at higher local temperatures;

a grid of bit and word lines connected to and providing for data access to the array, wherein both a thermal and electrical conductive path exists for each magnetic memory cell in the array to the grid; and

a plurality of thermally resistrictive links that electrically connect each respective magnetic memory cell in the array to corresponding points in the grid, and that increase the thermal resistance to heat generated in each of said magnetic memory cells;

wherein, during operation an active magnetic memory cell is caused to heat to a higher temperature than otherwise because the corresponding thermally resistrictive link interfers with its heat sinking to respective bit and word lines, and therefore switches magnetic states with less applied energy.

2. The MRAM of claim 1, wherein:

the plurality of thermally resistrictive links are each fabricated as metallic three-dimensional cones or pyramids.

3. The MRAM of claim 1, wherein:

the plurality of thermally resistrictive links are each fabricated as metallic vias with cross sections smaller that the adjacent bit or word line.

4. The MRAM of claim 1, wherein:

the plurality of thermally resistrictive links are each fabricated of a less thermally conductive material that the word or bit lines.

5. A method for improving a magnetic memory (MRAM) device comprising:

laying out an array of magnetic memory cells each with a magnetic data layer that can be switched between states, wherein said switching is more readily accomplished at higher local temperatures;

connecting a grid of bit and word lines to and providing for data access to the array, wherein both a thermal and electrical conductive path exists for each magnetic memory cell in the array to the grid; and

electrically connecting a plurality of thermally resistrictive links to each respective magnetic memory cell in the array that increase the thermal resistance to heat generated in each of said magnetic memory cells;

wherein, during operation an active magnetic memory cell is caused to heat to a higher temperature than otherwise because the corresponding thermally resistrictive link interfers with its heat sinking to respective bit and word lines, and therefore switches magnetic states with less applied energy.

6. A magnetic memory (MRAM) device comprising:

an array of magnetic memory cells each with a magnetic data layer that can be switched between states, wherein said switching is more readily accomplished at higher local temperatures;

a grid of bit and word lines connected to and providing for data access to the array, wherein both a thermal and electrical conductive path exists for each magnetic memory cell in the array to the grid; and

a plurality of thermally resistrictive rail facings that electrically connect each respective magnetic memory cell in the array to corresponding points in the grid, and that increase the thermal resistance to heat generated in each of said magnetic memory cells;

wherein, the plurality of thermally resistrictive rail facings are respectively disposed rail-for-rail on at least one of the bit and word lines in full contact along a row or column of the magnetic memory cells; and

wherein, during operation an active magnetic memory cell is caused to heat to a higher temperature than otherwise because the corresponding thermally resistrictive link interfers with its heat sinking to respective bit and word lines, and therefore switches magnetic states with less applied energy.

7. The MRAM of claim 6, wherein:

the plurality of thermally resistrictive rail facingsare each fabricated as reduced cross-sectional area wires compared to the word and bit lines.

8. The MRAM of claim 6, wherein:

the plurality of thermally resistrictive rail facingsare each fabricated with materials having reduced thermal conductivity compared to the word and bit lines.